A New Modulation Method to Reduce Common-Mode Voltages in Multilevel Inverters

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Abstract
This paper proposes a new modulation strategy for multilevel inverters, which selects voltage vectors that generate zero common-mode voltage in the load, working at low switching frequency. Experimental results confirm that the method is highly effective and simple to implement in a modern microprocessor. The voltage distortion (THD), the number of commutations and the linearity are also studied. Finally, it is concluded that the proposed strategy is highly suited for inverters with a high number of levels.

I. Introduction
The problem of common-mode voltage generation in inverter-fed AC machines has been extensively studied in the last years [1],[2],[3]. It has been shown that in Medium Voltage Adjustable Speed Drive applications, which are associated with critical processes, the common mode voltage is an important issue to consider [2],[4].

Common mode voltages are associated to shaft voltages and circulating leakage currents through parasitic capacitances between the motor windings, the rotor and the frame. The amplitude and number of these current spikes is determined by the dv/dt and the number of commutations present in the common mode voltage. These current spikes can cause premature motor bearings failures and electromagnetic interference (EMI) [3]. Some solutions are based on additional hardware like filters [2],[5] and other methods use more advanced modulation strategies which avoid the generation of common-mode voltages, some of them in the area of multilevel inverters [4],[6]. All these methods work with high switching frequency.

The problem of common-mode current spikes generation can be reduced by decreasing the switching frequency of the modulation strategy. This was accomplished in a previous paper developed by these authors, where the multilevel inverter operates with almost fundamental switching frequency [7].

This paper presents a control method, for high-level multilevel inverters, based on the space vector theory, which completely eliminates common-mode voltages. The following sections of the paper present the modulation algorithm and experimental results obtained with a 7-level and 11-level inverter.
II. Power Circuit Topology

Fig. 1 presents a general diagram for the power circuit of a multilevel inverter, which is applied in medium voltage drives. Each cell is composed of a non-controlled three-phase diode rectifier and a single phase H-type inverter, as shown in Fig. 2. Each single phase inverter generates an output voltage with three possible values $+V_{cc}$, 0 and $-V_{cc}$.

![Fig. 1. Power circuit of the cascade multilevel (CML) inverter.](image1)

![Fig. 2. Power circuit of a single cell.](image2)

III. Common Mode Voltage Generation in Vector Modulation Schemes

Three phase inverter output voltages can be represented by a space vector in a $x$-$y$ plane using the next transformation,

$$v = v_x + j \cdot v_y = \frac{2}{3} \cdot (v_{AN} + a \cdot v_{BN} + a^2 \cdot v_{CN})$$

(1)

where $v_{AN}$, $v_{BN}$, $v_{CN}$ are the voltages of terminals $A$, $B$ and $C$ with respect to the neutral $N$ and $a$ is the complex operator,
\[ a = -1/2 + j \cdot \sqrt{3}/2 \]  \hspace{1cm} (2)

Equation (1) can be expressed as a function of their real and imaginary components,

\[ \mathbf{v} = \mathbf{v}_x + j \cdot \mathbf{v}_y = \frac{1}{3} \cdot (2 \cdot \mathbf{v}_{AN} - \mathbf{v}_{BN} - \mathbf{v}_{CN}) + j \cdot \frac{1}{\sqrt{3}} \cdot (\mathbf{v}_{BN} - \mathbf{v}_{CN}) \]  \hspace{1cm} (3)

Considering the inverter of Fig. 1 with 3 cells per phase (7-level), each phase can generate 7 different voltages. Thus, the three-phase inverter has a total of \( 7 \cdot 7 \cdot 7 = 343 \) different output voltages \( \mathbf{v}_{AN}, \mathbf{v}_{BN}, \) and \( \mathbf{v}_{CN} \). These voltages generate 127 different voltage vectors represented by dots in Fig. 3. The production of space vectors with different combinations of phase voltages is known as redundancy. This redundancy property is due to the existence of zero sequence components in the phase voltages. For example, voltages \( (\mathbf{v}_{AN}, \mathbf{v}_{BN}, \mathbf{v}_{CN}) = (3\text{Vcc}, -\text{Vcc}, -2\text{Vcc}) \) and \( (\mathbf{v}_{AN}, \mathbf{v}_{BN}, \mathbf{v}_{CN}) = (2\text{Vcc}, -2\text{Vcc}, -3\text{Vcc}) \) generate the same vector, but the second set of voltages is clearly unbalanced \((\mathbf{v}_{AN} + \mathbf{v}_{BN} + \mathbf{v}_{CN} \neq 0)\).

The common mode voltage is defined as [1], [4]:

\[ \mathbf{v}_{cm} = \frac{1}{3} \cdot (\mathbf{v}_{AN} + \mathbf{v}_{BN} + \mathbf{v}_{CN}) \]  \hspace{1cm} (4)

Considering this definition, it is possible to find vectors generated by three phase voltages, which produce zero common mode voltage. These vectors are represented by a dot within a circle in Fig. 3 and are obtained with balanced phase voltages.

There are many papers that address this problem using only vectors with zero common mode voltage, however none of them have been developed in the context of low commutation frequency [4],[6].

**IV. Multilevel Sinusoidal PWM (MLSPWM)**

The classic Pulse Width Modulation method based on the comparison between a sinusoidal and carrier signals is commonly used in industrial cascaded inverter topologies [8] and, for this reason, it will be used as a reference to make an assessment with the proposed control strategy.

![Voltage vectors of a seven level inverter, including vectors with \( v_{cm} \) = 0 (*)](image)

Fig. 3. Voltage vectors of a seven level inverter, including vectors with \( v_{cm} \) = 0 (*).
The MLSPWM method has in one phase $C_n$ cascaded cells with their carriers shifted by an angle $\theta = \frac{360\degree}{2C_n}$, been compared in respect to the same reference signal in order to obtain a $2C_n+1$ level phase-neutral $N$ output voltage. The resulting load voltage has a sinusoidal multistep PWM waveform shown in Fig. 4, for a 7-level inverter.

Fig. 5 shows that this modulation method generates an important amount of common-mode voltages. The high quantity of commutations observed in $v_{cm}$ which can produce circulating currents through stray capacitances naturally formed in the converter-motor system [3], is especially detrimental.

![Fig. 4. 7-level inverter output voltage $v_{AN}$ with MLSPWM (simulation), modulation index $m=0.9$.](image1)

![Fig. 5. 7-level inverter common-mode voltage $v_{cm}$ with MLSPWM (simulation), modulation index $m=0.9$.](image2)
V. Proposed Modulation Algorithm

The main idea of the proposed strategy is to deliver the nearest voltage vector with respect to the reference vector $v_{ref}$, choosing only among vectors that generate zero common mode voltage, to the load. In order to select the appropriate vector with the information of the reference vector, the following simple algorithm has been developed:

Step 1. A transformation is applied to normalize the reference vector $v_{ref} = v_x + j v_y$.

$$
\begin{align*}
    v_{ref}' &= \frac{v_x}{V_{cc}} + j \cdot \frac{v_y}{V_{cc}/\sqrt{3}} \\
    \text{(5)}
\end{align*}
$$

In addition, the transformation of equation (5) changes the position of the candidate space vectors with $v_{cm}=0$ to integer values, as can be seen in Fig. 6.

Step 2. There are two vectors with $v_{cm}=0$ in each rectangle of the complex plane. These vectors are named $v'_h$ and $v'_l$ for the shaded rectangle where the reference $v_{ref}'$ belongs to (see Fig 6). The nearest vector is selected comparing the distances of each candidate vector $v'_h$ and $v'_l$ with respect to $v_{ref}'$, using the following equations:

$$
\begin{align*}
    d_h &= \sqrt{(3 \cdot (\text{Re}(v_{ref}') - \text{Re}(v_h'))^2 + (\text{Im}(v_{ref}') - \text{Im}(v_h'))^2)} \\
    d_l &= \sqrt{(3 \cdot (\text{Re}(v_{ref}') - \text{Re}(v_l'))^2 + (\text{Im}(v_{ref}') - \text{Im}(v_l'))^2)} \\
    \text{(6)} \quad \text{(7)}
\end{align*}
$$

The decision between $v'_h$ or $v'_l$ is done by

$$
\begin{align*}
    &\text{if } d_h \leq d_l \text{ then } v_{sel} = v_h' \\
    &\text{else } v_{sel} = v_l' \\
    \text{(8)}
\end{align*}
$$

![Normalized space vectors](image-url)
Step 3. An inverse transformation is applied to the selected vector $v_{sel}$ to generate three-phase output voltages with zero common mode voltage. This transformation is given by

\[
\begin{align*}
    v_{AN} &= \text{round}(\text{Re}(v_{sel})) \\
    v_{BN} &= \frac{(\text{Im}(v_{sel}) - 3 \cdot \text{Re}(v_{sel}))}{2} + v_{AN} \\
    v_{CN} &= \frac{-(\text{Im}(v_{sel}) - 3 \cdot \text{Re}(v_{sel}))}{2} + v_{AN}
\end{align*}
\]

(9)

VI. Experimental Results

The modulation strategy was applied in a multicell inverter prototype, with 3 and 5 cells in each phase. The 16 bits fixed point DSP controller ADMC331 was employed to transform the reference vector and control the inverter to synthesize the appropriate output voltage. In this hardware implementation, the execution time to generate the output voltage was 6 only (us).

Fig. 7-a) represents the phase voltage $v_{AN}$ in a 7-level inverter controlled by the proposed method, operating with a modulation index of $m=0.9$ and fundamental frequency of 50 (Hz). This result has a similar fundamental voltage to the one originated by the MLSPWM method, shown in fig. 4. It must be noticed that number of commutations in the load voltage in fig. 7 is drastically reduced with respect to the voltage of figure 4. Fig. 7-b) shows that the proposed method effectively eliminates the common mode voltage in comparison to the values observed in fig. 5.

Fig. 8 presents experimental results obtained in a 11-level inverter, which has 5 cells in series connection per phase. The waveform of fig 8-a) corresponds to the output voltage $v_{AN}$ with a modulation index of $m=0.9$ and an output frequency of 50 (Hz). The resulting voltage is highly sinusoidal and the common mode voltage is also eliminated.

![Fig. 7. 7-level inverter with proposed method (experimental, $m=0.9$): a) output voltage $v_{AN}$ (50 (V/div)); b) $v_{cm}$ (10 (V/div)) , time scale: 5 (ms/div).](image)
An 11-level inverter has a lot more voltage vectors to be selected from than a 7-level inverter. However, the execution time of the algorithm to select a voltage vector is the same for both inverters.

VII. Linear Range and THD Analysis

The use of vectors with $v_{cm}=0$ increases the distance between $v_{ref}$ and the vectors effectively delivered by the inverter. This means an increase in the error of the generated voltage with respect to the reference.

Fig. 9 represents the relationship between the amplitude of the fundamental load voltage $a_1$ and the modulation index $m$, which must be linear for a good modulation method. In this paper, the modulation index is defined as,

$$m = \frac{|v_{ref}| \cdot \sqrt{3}}{2 \cdot C_n \cdot Vcc}$$

where $C_n$ is the cell number in each phase. It can be observed that the proposed method does not have a linear relationship between $a_1$ and $m$, which is not desirable. This fact is a natural result of the reduction in the number of available space vectors. This problem is less severe in inverters with a higher number of levels. Fig 10 shows that an 11-level inverter has a much better relationship between $a_1$ and $m$.

Another important aspect to consider in the evaluation of this modulation method is the Total Harmonic Distortion (THD) of the load voltage. Fig 11 shows that the THD increases with decreasing modulation index $m$, which is normal for all modulation methods. This figure also shows that this method has a comparable THD with respect to the MLSPWM strategy. The reason for this effect is that the MLSPWM carrier based method does not fully utilize the nearest available phase voltage with respect to a sinusoidal reference, whereas the vector method does. However, the performance of the carrier based PWM method is superior considering the harmonic currents. This is a logical consequence of the low-pass filtering capability of every AC machine drive.
Fig. 9. Fundamental load voltage ($a_1$) versus modulation index ($m$) in a 7 level inverter working with the proposed modulation scheme. ($1 \text{ (pu)} = \frac{6 \cdot V_{cc}}{\sqrt{3}}$).

Fig. 10. Fundamental load voltage ($a_1$) versus modulation index ($m$) in an 11 level inverter working with the proposed modulation scheme. ($1 \text{ (pu)} = \frac{10 \cdot V_{cc}}{\sqrt{3}}$).
Fig. 11. Load Voltage THD comparison in an 11 level inverter for different modulation indices.

VIII. Conclusions

The classical MLSPWM widely used in the industry presents a large amount of commutations in the common mode voltage, consequently producing a large quantity of current spikes.

The new modulation strategy proposed in this paper eliminates common-mode voltages in multilevel inverters, selecting only space voltage vectors with \( v_{cm} = 0 \), operating with almost fundamental switching frequency. This method has a comparable voltage THD with respect to the MLSPWM, despite the fact that not all possible vectors are used. The reason for this result is that the space vector control proposed in this paper selects the nearest voltage vector with respect to a reference.

The authors believe that this method is suitable for inverters with 7 or more levels, otherwise the generated voltages and currents will have high levels of distortion.

IX. References


